UNIVERSITY COLLEGE OF ENGINEERING (Autonomous) OSMANIA UNIVERSITY, HYDERABAD

M.E. (E.C.E) II - Semester (Regular & PTPG) Main Examination September 2015 Examination Centre: Department of ECE, UCE (A), O.U.

EXAMINATION TIME TABLE

Time: 2.00 PM to 5.00 PM

	Digital Systems		Systems & Signal Processing		Microwave & Radar Engineering		Embedded Systems and VLSI Design
Date and Day	Regular II-Semester	PTPG II-Semester	Regular II-Semester	PTPG II-Semester	Regular II-Semester	PTPG II-Semester	Regular II-Semester
14-09-2015 MONDAY	Advanced Digital Design with Verilog HDL	=====	Optimal Control Theory	Digital Spectral Analysis	Global Navigational Satellite Systems	Global Navigational Satellite Systems	Advanced Digital Design with Verilog HDL
16-09-2015 WEDNESDAY	Data & Computer Communication Networks	Data & Computer Communication Networks	====	====	Microwave Integrated Circuits	Microwave Integrated Circuits	=====
18-09-2015 FRIDAY	Low Power VLSI Design	=====	Optical Fiber Communication Systems	====	Microwave Solid State Devices		Low Power VLSI Design
21-09-2015 MONDAY	Real Time Operating System		Image & Video Processing	====	Microwave Antennas	Microwave Antennas	Real Time Operating System
23-09-2015 WEDNESDAY	VLSI Design & Technology	VLSI Design & Technology	Adaptive Signal Processing	Adaptive Signal Processing	Electromagnetic Interference and Compatibility	=====	VLSI Physical Design
25-09-2015 FRIDAY	=====	=====	Engineering Mathematics	====	Optimization Techniques	=====	DSP Processors Architecture
28-09-2015 MONDAY	Coding Theory & Techniques	Coding Theory & Techniques	Coding Theory & Techniques	Coding Theory & Techniques	Phased Array Radar	=====	VLSI Technology

Note: 1. This Time-Table is also applicable for Pre-Ph.D. students.

2. Backlog students are eligible to appear without Re-registration of the subjects as per this Timetable.

DIRECTOR OF EVALUATION EXAMINATION CELL